TREX-S2

Stratix II FPGA Module

Data Book

TREX-S2

Document Version 1.3 NOV. 29, 2006 by Terasic

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Chapter 1

Introduction

TREX-S2 is an innovative FPGA module which enables users to use ALL the powerful features of Altera StratixII FPGAs without having to worry about how to design the complex circuits for power supply and configurations; Also, TREX-S2 users can access all the available FPGA IOs without having to worry about how to create and manufacture the complex BGA PCB board.

With the increasing demand in using large FPGA with bigger BGA package for many applications, FPGA vendors must find out a way for customers to adopt FPGA devices quickly without forcing the customers to know all the details in the BGA PCB design and manufacturing.

With the innovative and flexible feature set provided in TREX-S2 module, using large Altera Stratix II FPGA devices can be as simple as using an Intel CPU Pentium Module on a user main board.

Features

Figure 1.1 shows the photo of the TREX-S2 FPGA module. The important features are listed below:

- ✓ Altera Stratix II FPGA (60-180) with 1020 FBGA package
- ✓ Provides **695 Free** IO pins via high-speed connectors.
- ✓ **12 connectors (3 in each side)** to ease the layout design of users' own motherboards.
- ✓ Portable – can be easily put on various motherboards to increase the reusability of the FPGA module.
- ✓ **All bank VCCIO can be adjusted** separately to support various interface protocols.
- ✓ Flexible clocking system (up to 420Mhz performance)
- ✓ Support various reconfiguration options:
  - JTAG and JTAG Chain
  - AS PROG from EPCS16/EPCS64 configuration devices
- ✓ Provides TREX-S2-TMA motherboard **schematic and gerber files** for

users to create their own motherboards.

✓ Provide various optional motherboards for different purpose.

Figure 1.1. The top side of the TREX-S2 FPGA Module

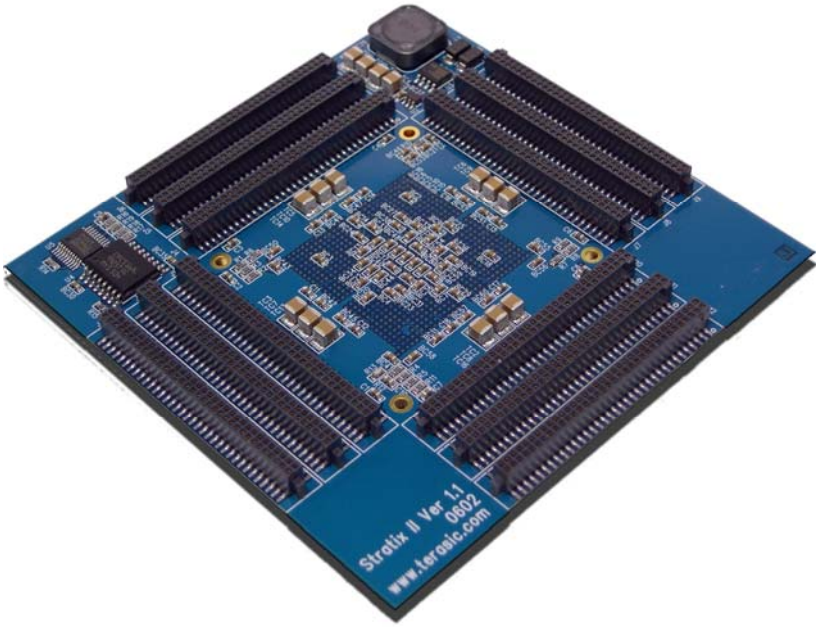

Figure 1.2. The bottom side of the TREX-S2 FPGA Module

TREX-S2 Selection Guide

TREX-S2 module has the following naming structure: **TREX-S2-XY-N,** where **XY** is the type of the Stratix II devices and **N** is the speed grade selected. The available product portfolio is listed below:

Ordering Code	FPGA Devices	Speed Grade	FPGA Internal RAM	User I/O	#of LEs	Lead Time
TREX-S2-60-5	Stratix II 60	5	~2.5Mb	679	~60K	In Stock
TREX-S2-60-4	Stratix II 60	4	~2.5Mb	679	~60K	In Stock
TREX-S2-60-3	Stratix II 60	3	~2.5Mb	679	~60K	In Stock
TREX-S2-180-5	Stratix II 180	5	~9.3Mb	695	~180K	In Stock
TREX-S2-180-3	Stratix II 180	3	~9.3Mb	695	~180K	In Stock

Figure 1.3 Terasic TREX-S2 Module Part Number

TREX-S2 Motherboard Selection Guide

TREX-S2 module has a series of motherboards designed for various applications. The available product portfolio is listed below. To request the detailed specification of a TREX-S2 Motherboard, please send email to support@terasic.com. Figure 1.5 shows the TREX-S2 module with TREX-S2-TMA motherboard. Figure 1.6 shows the TREX-S2 module with TREX-S2-TMB motherboard.

Product Code	Applications	Listing Price	Spec File Name
TREX-S2-TMA	Prototyping	$325	TREXS2_TMA.pdf
TREX-S2-TMB	Prototyping with DDRII, SRAM, SDRAM	$395	TREXS2_TMB.pdf

Figure 1.4 Terasic TREX-S2 Motherboard Part Number

Figure 1.5 Terasic TREX-S2 Module with TREX-S2_TMA Motherboard

Figure 1.6 Terasic TREX-S2 Module with TREX-S2_TMB Motherboard

USB Blaster Cable is included

To shorten the downloading time of large FPGA, ONE USB-Blaster cable will be included with each motherboard for users free of charge. Figure 1.7 shows the photo of the USB-Blaster download cable.

Figure 1.7 USB-Blaster download cable

Getting Help

Here are some places to get help if you encounter any problem:

- ✓ Email to support@terasic.com
- ✓ Taiwan & China: +886-3-550-8800
- ✓ Korea : +82-2-512-7661
- ✓ Japan: +81-428-77-7000
- ✓ English Support Line: +1-403-512-1336

Chapter 2

Architecture

This chapter describes the architecture of the TREX-S2 module including block diagram, connectors, and clocking system.

The Block Diagram

The block diagram of the TREX-S2 module is described in Figure 2.1.

- ✓ 840 pins are connected to four connector groups – top, bottom, left, and right connector groups.
- ✓ Each connector group consists of 3 connectors.
- ✓ VCCINT (1.2V) is provided onboard – no need to use external VCCINT
- ✓ Provides configuration device (EPCS16/EPCS64) on board

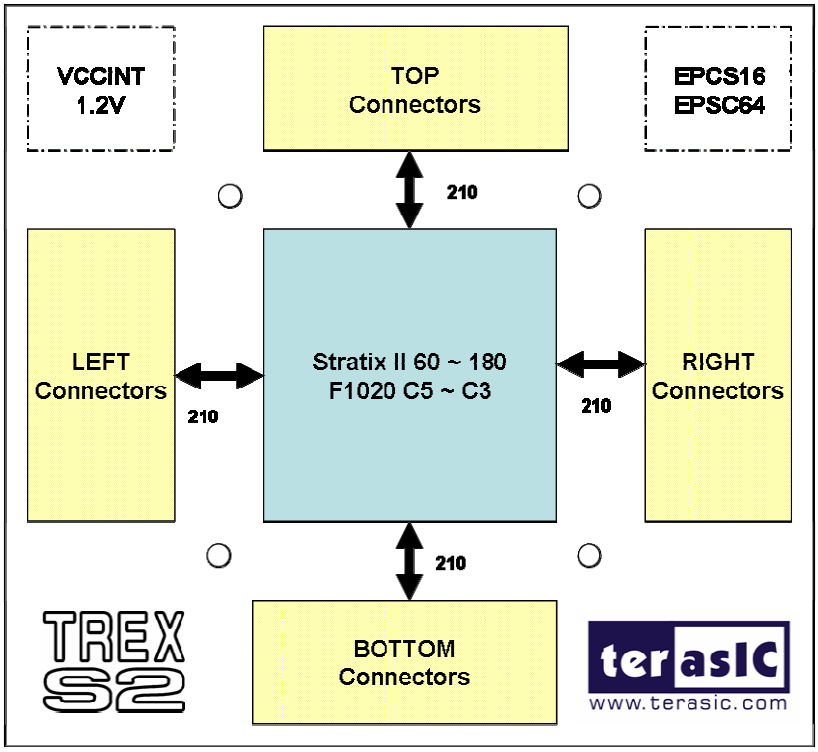

Figure 2.1 Terasic TREX-S2 Module Block Diagram

Connectors

Figure 2.2 shows the Connector Diagram of the TREX-S2

- ✓ All **840** pins are connected to four connector groups – top, bottom, left, and right. Each connector group has 210 pins connected to the FPGA, VCCIO, and GND.
- ✓ Each connector group consists of 3 connectors (**RIGHT**: J1, J2, J3; **TOP**: J4, J5, J6; **LEFT**: J7, J8, J9; **BOTTOM**: J10, J11, J112).

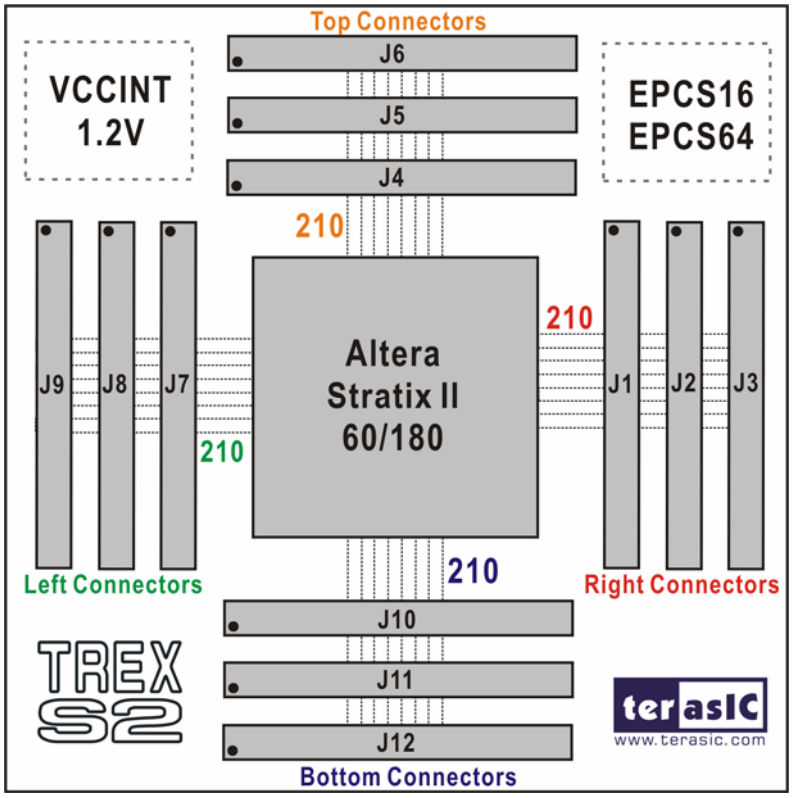

Figure 2.2. TREX-S2 Connector Architecture

Important Pin Assignment

Bank Arrangement

- ✓ J1, J2, J3 connect to Stratix II I/O Bank 1 & 2
- ✓ J3, J4, J5 connect to Stratix II I/O Bank 3 & 4.
- ✓ J7, J8, J9 connect to Stratix II I/O Bank 5 & 6
- ✓ J10, J11, J12 connect to Stratix II I/O Bank 7 & 8.
- ✓ ALL the I/O pins in the same bank must be configured to the same interface standard (LVTTL, SSTL etc)

Configuration Methods

- ✓ Provides EPCS16/64 Serial Configuration device for AS Mode programming
- ✓ Allows JTAG mode to download SOF directly to the FPGA device.
- ✓ Configuration Pins
  - ■ **nIO_PULLUP** is low by default (via a 4.7K pull-down resistor). This setup will force ALL the dual-purpose pins in the configuration pin group to remain the same level as previous configured during the reconfiguration downloading process. If these dual-purpose pins were configured as output pins with a pre-defined value, the reconfiguration will fail. **Therefore, we strongly suggest users NOT to use ANY of the dual-purpose pins in the configuration pin group as GPIO. In the case of any damage occurred to any of the pins required for configuration, the FPGA device will no longer be reconfigured.**
  - ■ **PORSEL** is low by default (via a 4.7K pull-down resistor). This is to select the POR (Power ON Reset) time to 12 ms, instead of 100ms when PORSEL pin is set to high.
  - ■ **MSEL0 – MSEL3** is floating (users' main board must connect these pins to **HIGH** or **LOW** according to the preferred configuration method selected), please refer to the following Altera literature on configuration scheme: http://www.altera.com/literature/hb/stx2/stx2_sii52007.pdf

VCC33, VCCINT, Bank VCCIO, Bank VREF,

- ✓ **VCC33:** A user input power supplier to provide power to the TREX-S2 Module.
- ✓ **VCCINT:** FPGA internal logic array voltage supply pins. All VCCINT pins must be connected to 1.2 V.
- ✓ **Bank VCCIO**: FPGA I/O supply voltage pins for banks 1 through 8. Each

bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5 V, 1.8 V, 2.5 V, 3.3-V PCI, and 3.3-V PCI-X I/O standards.

- ✓ **Bank VREF**: Input reference voltage for each I/O bank. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for that bank. All of the VREF pins within a bank are shorted together. If VREF pins are not used, designers should connect them to either VCC or GND.

We used different colors to annotate each pin in each connector. The color annotation table is listed below. This table is important for users to understand the pin assignment of the connectors in the next section.

GREEN	**Power GND**
RED	**VCCINT DC/DC Power**
PINK	**Bank VCCIO**
ROSE	**Bank VREF**
YELLOW	**Input Only**
BLUE	**Configuration / Multi Function IO**
PURPLE	**StratixII 60 N.C.**
WHITE	**GPIO**

Detailed Connector Assignment

Please refer to the Color Annotation Table listed in previous section for better understanding.

J1 Bank1 and Bank2							
PIN	PinOut	StratixII 180	StratixII 60	PIN	PinOut	StratixII 180	StratixII 60
1	GND	GND	GND	2	GND	GND	GND
3	D29	FPLL7CLKn, Input	FPLL7CLKn, Input	4	D30	FPLL7CLKp, Input	FPLL7CLKp, Input
5	VREF	VREF	VREF	6	GND	GND	GND
7	D31	DIFFIO_RX62n	DIFFIO_RX40n	8	D32	DIFFIO_RX62p	DIFFIO_RX40p
9	E31	DIFFIO_RX57n	DIFFIO_RX35n	10	E32	DIFFIO_RX57p	DIFFIO_RX35p
11	F31	DIFFIO_RX56n	DIFFIO_RX34n	12	F32	DIFFIO_RX56p	DIFFIO_RX34p
13	G31	DIFFIO_RX55n	DIFFIO_RX33n	14	G32	DIFFIO_RX55p	DIFFIO_RX33p
15	H31	DIFFIO_RX54n	DIFFIO_RX32n	16	H32	DIFFIO_RX54p	DIFFIO_RX32p
17	J31	DIFFIO_RX53n	DIFFIO_RX31n	18	J32	DIFFIO_RX53p	DIFFIO_RX31p
19	K31	DIFFIO_RX51n	DIFFIO_RX29n	20	K32	DIFFIO_RX51p	DIFFIO_RX29p
21	L31	DIFFIO_RX47n	DIFFIO_RX25n	22	L32	DIFFIO_RX47p	DIFFIO_RX25p
23	M31	DIFFIO_RX45n	DIFFIO_RX23n	24	M32	DIFFIO_RX45p	DIFFIO_RX23p
25	P31	DIFFIO_RX44n	DIFFIO_RX22n	26	P32	DIFFIO_RX44p	DIFFIO_RX22p
27	R30	DIFFIO_RX43n	DIFFIO_RX21n	28	R31	DIFFIO_RX43p	DIFFIO_RX21p
29	T29	CLK1n, Input	CLK1n, Input	30	T30	CLK1p, Input	CLK1p, Input
31	T31	CLK0n/	CLK0n/	32	T32	CLK0p/	CLK0p/
33	VCC33	DC/DC POWER	DC/DC POWER	34	VCC33	DC/DC POWER	DC/DC POWER
35	GND	GND	GND	36	GND	GND	GND
37	VCCB12	VCCIO	VCCIO	38	VCCB12	VCCIO	VCCIO
39	U31	CLK2n/	CLK2n/	40	U32	CLK2p/	CLK2p/
41	U29	CLK3n, Input	CLK3n, Input	42	U30	CLK3p, Input	CLK3p, Input
43	V30	DIFFIO_RX42n	DIFFIO_RX20n	44	V31	DIFFIO_RX42p	DIFFIO_RX20p
45	W31	DIFFIO_RX41n	DIFFIO_RX19n	46	W32	DIFFIO_RX41p	DIFFIO_RX19p
47	AA31	DIFFIO_RX40n	DIFFIO_RX18n	48	AA32	DIFFIO_RX40p	DIFFIO_RX18p
49	AB31	DIFFIO_RX38n	DIFFIO_RX16n	50	AB32	DIFFIO_RX38p	DIFFIO_RX16p
51	AC31	DIFFIO_RX34n	DIFFIO_RX12n	52	AC32	DIFFIO_RX34p	DIFFIO_RX12p
53	AD31	DIFFIO_RX32n	DIFFIO_RX10n	54	AD32	DIFFIO_RX32p	DIFFIO_RX10p
55	AE31	DIFFIO_RX31n	DIFFIO_RX9n	56	AE32	DIFFIO_RX31p	DIFFIO_RX9p
57	AF31	DIFFIO_RX30n	DIFFIO_RX8n	58	AF32	DIFFIO_RX30p	DIFFIO_RX8p
59	AG31	DIFFIO_RX29n	DIFFIO_RX7n	60	AG32	DIFFIO_RX29p	DIFFIO_RX7p
61	AH31	DIFFIO_RX26n	DIFFIO_RX4n	62	AH32	DIFFIO_RX26p	DIFFIO_RX4p
63	AJ31	DIFFIO_RX24n	DIFFIO_RX2n	64	AJ32	DIFFIO_RX24p	DIFFIO_RX2p
65	VREF	VREF.	VREF	66	GND	GND	GND
67	AJ29	FPLL8CLKn, Input	FPLL8CLKn, Input	68	AJ30	FPLL8CLKp, Input	FPLL8CLKp, Input
69	GND	GND	GND	70	GND	GND	GND

J2 Bank1 and Bank2							
PIN	PinOut	StratixII 180	StratixII 60	PIN	PinOut	StratixII 180	StratixII 60
1	GND	GND	GND	2	GND	GND	GND
3	E29	DIFFIO_RX63n	DIFFIO_RX39n	4	E30	DIFFIO_RX63p	DIFFIO_RX39p
5	G27	DIFFIO_RX64n	N.C.	6	G28	DIFFIO_RX64p	N.C.
7	H27	DIFFIO_TX64n	DIFFIO_TX40n	8	H28	DIFFIO_TX64p	DIFFIO_TX40p
9	J26	DIFFIO_TX62n	DIFFIO_TX39n	10	J27	DIFFIO_TX62p	DIFFIO_TX39p
11	K24	DIFFIO_TX61n	DIFFIO_TX41n	12	K25	DIFFIO_TX61p	DIFFIO_TX41p
13	K29	DIFFIO_RX52n	DIFFIO_RX30n	14	K30	DIFFIO_RX52p	DIFFIO_RX30p
15	L25	DIFFIO_TX60n	DIFFIO_TX35n	16	L26	DIFFIO_TX60p	DIFFIO_TX35p
17	M22	DIFFIO_TX57n	DIFFIO_TX36n	18	M23	DIFFIO_TX57p	DIFFIO_TX36p
19	M26	DIFFIO_TX56n	DIFFIO_TX32n	20	M27	DIFFIO_TX56p	DIFFIO_TX32p
21	N24	DIFFIO_TX55n	DIFFIO_TX31n	22	N25	DIFFIO_TX55p	DIFFIO_TX31p
23	N28	DIFFIO_RX49n	DIFFIO_RX27n	24	N29	DIFFIO_RX49p	DIFFIO_RX27p
25	P24	DIFFIO_TX49n	DIFFIO_TX27n	26	P25	DIFFIO_TX49p	DIFFIO_TX27p
27	P28	DIFFIO_TX51n	DIFFIO_TX29n	28	P29	DIFFIO_TX51p	DIFFIO_TX29p
29	R26	DIFFIO_TX48n	DIFFIO_TX26n	30	R27	DIFFIO_TX48p	DIFFIO_TX26p
31	T22	DIFFIO_TX43n	DIFFIO_TX21n	32	T23	DIFFIO_TX43p	DIFFIO_TX21p
33	VCC33	DC/DC POWER	DC/DC POWER	34	VCC33	DC/DC POWER	DC/DC POWER
35	GND	GND	GND	36	GND	GND	GND
37	VCCB12	VCCIO	VCCIO	38	VCCB12	VCCIO	VCCIO
39	U22	DIFFIO_TX42n	DIFFIO_TX20n	40	U23	DIFFIO_TX42p	DIFFIO_TX20p
41	V23	DIFFIO_TX39n	DIFFIO_TX17n	42	V24	DIFFIO_TX39p	DIFFIO_TX17p
43	W24	DIFFIO_TX36n	DIFFIO_TX14n	44	W25	DIFFIO_TX36p	DIFFIO_TX14p
45	W28	DIFFIO_TX38n	DIFFIO_TX16n	46	W29	DIFFIO_TX38p	DIFFIO_TX16p
47	Y26	DIFFIO_TX35n	DIFFIO_TX13n	48	Y27	DIFFIO_TX35p	DIFFIO_TX13p
49	Y30	DIFFIO_RX39n	DIFFIO_RX17n	50	Y31	DIFFIO_RX39p	DIFFIO_RX17p
51	AA26	DIFFIO_TX34n	DIFFIO_TX12n	52	AA27	DIFFIO_TX34p	DIFFIO_TX12p
53	AB23	DIFFIO_TX25n	DIFFIO_TX3n	54	AB24	DIFFIO_TX25p	DIFFIO_TX3p
55	AB27	DIFFIO_RX33n	DIFFIO_RX11n	56	AB28	DIFFIO_RX33p	DIFFIO_RX11p
57	AC24	DIFFIO_TX24n	DIFFIO_TX4n	58	AC25	DIFFIO_TX24p	DIFFIO_TX4p
59	AC29	DIFFIO_RX28n	N.C.	60	AC30	DIFFIO_RX28p	N.C.
61	AD26	DIFFIO_TX31n	DIFFIO_TX9n	62	AD27	DIFFIO_TX31p	DIFFIO_TX9p
63	AE25	DIFFIO_TX22n	DIFFIO_TX1n	64	AE26	DIFFIO_TX22p	DIFFIO_TX1p
65	AE29	DIFFIO_RX25n	DIFFIO_RX6n	66	AE30	DIFFIO_RX25p	DIFFIO_RX6p
67	AG29	DIFFIO_RX22n	DIFFIO_RX3n	68	AG30	DIFFIO_RX22p	DIFFIO_RX3p
69	GND	GND	GND	70	GND	GND	GND

J3 Bank1 and Bank2							
PIN	PinOut	StratixII 180	StratixII 60	PIN	PinOut	StratixII 180	StratixII 60
1	GND	GND	GND	2	GND	GND	GND
3	F29	DIFFIO_RX61n	DIFFIO_RX38n	4	F30	DIFFIO_RX61p	DIFFIO_RX38p
5	G29	DIFFIO_RX60n	DIFFIO_RX37n	6	G30	DIFFIO_RX60p	DIFFIO_RX37p
7	H29	DIFFIO_RX59n	DIFFIO_RX36n	8	H30	DIFFIO_RX59p	DIFFIO_RX36p
9	J29	DIFFIO_RX58n	N.C.	10	J30	DIFFIO_RX58p	N.C.
11	K26	DIFFIO_TX63n	DIFFIO_TX37n	12	K27	DIFFIO_TX63p	DIFFIO_TX37p
13	L23	DIFFIO_TX59n	DIFFIO_TX38n	14	L24	DIFFIO_TX59p	DIFFIO_TX38p
15	L29	DIFFIO_RX50n	DIFFIO_RX28n	16	L30	DIFFIO_RX50p	DIFFIO_RX28p
17	M24	DIFFIO_TX58n	DIFFIO_TX34n	18	M25	DIFFIO_TX58p	DIFFIO_TX34p
19	M29	DIFFIO_RX48n	DIFFIO_RX26n	20	M30	DIFFIO_RX48p	DIFFIO_RX26p
21	N26	DIFFIO_TX52n	DIFFIO_TX30n	22	N27	DIFFIO_TX52p	DIFFIO_TX30p
23	N30	DIFFIO_RX46n	DIFFIO_RX24n	24	N31	DIFFIO_RX46p	DIFFIO_RX24p
25	P26	DIFFIO_TX50n	DIFFIO_TX28n	26	P27	DIFFIO_TX50p	DIFFIO_TX28p
27	R24	DIFFIO_TX46n	DIFFIO_TX24n	28	R25	DIFFIO_TX46p	DIFFIO_TX24p
29	R28	DIFFIO_TX45n	DIFFIO_TX23n	30	R29	DIFFIO_TX45p	DIFFIO_TX23p
31	T27	DIFFIO_TX44n	DIFFIO_TX22n	32	T28	DIFFIO_TX44p	DIFFIO_TX22p
33	VCC33	DC/DC POWER	DC/DC POWER	34	VCC33	DC/DC POWER	DC/DC POWER
35	GND	GND	GND	36	GND	GND	GND
37	VCCB12	VCCIO	VCCIO	38	VCCB12	VCCIO	VCCIO
39	U27	DIFFIO_TX41n	DIFFIO_TX19n	40	U28	DIFFIO_TX41p	DIFFIO_TX19p
41	V28	DIFFIO_TX40n	DIFFIO_TX18n	42	V29	DIFFIO_TX40p	DIFFIO_TX18p
43	W26	DIFFIO_TX37n	DIFFIO_TX15n	44	W27	DIFFIO_TX37p	DIFFIO_TX15p
45	Y24	DIFFIO_TX33n	DIFFIO_TX11n	46	Y25	DIFFIO_TX33p	DIFFIO_TX11p
47	Y28	DIFFIO_RX36n	DIFFIO_RX14n	48	Y29	DIFFIO_RX36p	DIFFIO_RX14p
49	AA24	DIFFIO_TX28n	DIFFIO_TX6n	50	AA25	DIFFIO_TX28p	DIFFIO_TX6p
51	AA29	DIFFIO_RX37n	DIFFIO_RX15n	52	AA30	DIFFIO_RX37p	DIFFIO_RX15p
53	AB25	DIFFIO_TX27n	DIFFIO_TX5n	54	AB26	DIFFIO_TX27p	DIFFIO_TX5p
55	AB29	DIFFIO_RX35n	DIFFIO_RX13n	56	AB30	DIFFIO_RX35p	DIFFIO_RX13p
57	AC26	DIFFIO_TX30n	DIFFIO_TX8n	58	AC27	DIFFIO_TX30p	DIFFIO_TX8p
59	AD24	DIFFIO_TX23n	DIFFIO_TX2n	60	AD25	DIFFIO_TX23p	DIFFIO_TX2p
61	AD29	DIFFIO_RX27n	N.C.	62	AD30	DIFFIO_RX27p	N.C.
63	AE27	DIFFIO_TX21n	DIFFIO_TX0n	64	AE28	DIFFIO_TX21p	DIFFIO_TX0p
65	AF29	DIFFIO_RX23n	DIFFIO_RX5n	66	AF30	DIFFIO_RX23p	DIFFIO_RX5p
67	AH29	DIFFIO_RX21n	DIFFIO_RX1n	68	AH30	DIFFIO_RX21p	DIFFIO_RX1p
69	GND	GND	GND	70	GND	GND	GND

J4 Bank3 and Bank4							
PIN	PinOut	StratixII 180	StratixII 60	PIN	PinOut	StratixII 180	StratixII 60
1	GND	GND	GND	2	GND	GND	GND
3	B4	DQ0T	DQ0T	4	A4	DQ0T	DQ0T
5	VREF	VREF	VREF	6	GND	GND	GND
7	B5	DQS1T/DQ0T	DQS1T/DQ0T	8	A5	DQ1T	DQ1T
9	B6	DQSn1T	DQSn1T	10	A6	DQ1T	DQ1T
11	B7	DQ2T	DQ2T	12	A7	DQ2T	DQ2T
13	B8	DQS3T/DQ1T	DQS3T/DQ1T	14	A8	DQ3T	DQ3T
15	B9	DQSn3T	DQSn3T	16	A9	DQ3T	DQ3T
17	B10	DQ5T	DQ5T	18	A10	DQ5T	DQ5T
19	B11	DQ7T	DQ7T	20	A11	DQ7T	DQ7T
21	B12	DQSn7T	DQSn7T	22	A12	DQ7T	DQ7T
23	C13	DQS9T/DQ4T	DQS9T/DQ4T	24	B13	DQSn9T	DQSn9T
25	B14	DQ9T	DQ9T	26	A14	DQ9T	DQ9T
27	C15	PLL5_OUT0n	PLL5_OUT0n	28	B15	PLL5_OUT0p	PLL5_OUT0p
29	F16	CLK13n	CLK13n	30	E16	CLK13p	CLK13p
31	B16	CLK12n	CLK12n	32	A16	CLK12p	CLK12p
33	VCC33	DC/DC POWER	DC/DC POWER	34	VCC33	DC/DC POWER	DC/DC POWER
35	GND	GND	GND	36	GND	GND	GND
37	VCCB34	VCCIO	VCCIO	38	VCCB34	VCCIO	VCCIO
39	B17	CLK14n	CLK14n	40	A17	CLK14p	CLK14p
41	D17	CLK15n	CLK15n	42	C17	CLK15p	CLK15p
43	C18	PLL11_OUT0n	PLL11_OUT0n	44	B18	PLL11_OUT0p	PLL11_OUT0p
45	B19	PLL11_FBn/OUT2n	PLL11_FBn/OUT2n	46	A19	PLL11_FBp/OUT2p	PLL11_FBp/OUT2p
47	C20	DQ10T	DQ10T	48	B20	DQ10T	DQ10T
49	B21	DQS11T/DQ5T	DQS11T/DQ5T	50	A21	DQ11T	DQ11T
51	B22	DQSn11T	DQSn11T	52	A22	DQ11T	DQ11T
53	B23	DQS13T/DQ6T	DQS13T/DQ6T	54	A23	DQ13T	DQ13T
55	B24	DQSn13T	DQSn13T	56	A24	DQ13T	DQ13T
57	B25	DQS14T	DQS14T	58	A25	DQ14T	DQ14T
59	B26	DQSn14T	DQSn14T	60	A26	DQ14T	DQ14T
61	B27	DQS16T/DQ3T	DQS16T/DQ3T	62	A27	DQ16T	DQ16T
63	B28	DQSn16T	DQSn16T	64	A28	DQ16T	DQ16T
65	VREF	VREF	VREF	66	GND	GND	GND
67	B29	DQ17T	DQ17T	68	A29	DQ17T	DQ17T
69	GND	GND	GND	70	GND	GND	GND

J5 Bank3 and Bank4							
PIN	PinOut	StratixII 180	StratixII 60	PIN	PinOut	StratixII 180	StratixII 60
1	GND	GND	GND	2	GND	GND	GND
3	B2	MSEL0	MSEL0	4	C3	TDO	TDO
5	E5	DQ0T	DQ0T	6	D5	DQ0T	DQ0T
7	F6	MSEL1	MSEL1	8	E6	DQ2T	DQ2T
9	E7	DQ2T	DQ2T	10	C8	DQ3T	DQ3T
11	D8	DQ4T	DQ4T	12	C9	DQ3T	DQ3T
13	D10	DQ5T	DQ5T	14	C10	DQS5T/DQ2T	DQS5T/DQ2T
15	J10	MSEL2	MSEL2	16	H10	MSEL3	MSEL3
17	F11	DQS6T	DQS6T	18	E11	DQ6T	DQ6T
19	D12	DQ7T	DQ7T	20	C12	DQS7T/DQ3T	DQS7T/DQ3T
21	J12	Column I/O	Column I/O	22	H12	Column I/O	Column I/O
23	G13	DQ8T	DQ8T	24	F13	DQ8T	DQ8T
25	E14	DQSn8T	DQSn8T	26	D14	DQ9T	DQ9T
27	K14	Column I/O	Column I/O	28	J14	Column I/O	Column I/O
29	J15	Column I/O	Column I/O	30	F15	DQ8T	DQ8T
31	D16	PLL5_OUT1n	PLL5_OUT1n	32	C16	PLL5_OUT1p	PLL5_OUT1p
33	VCC33	DC/DC POWER	DC/DC POWER	34	VCC33	DC/DC POWER	DC/DC POWER
35	GND	GND	GND	36	GND	GND	GND
37	VCCB34	VCCIO	VCCIO	38	VCCB34	VCCIO	VCCIO
39	F17	ASDO	ASDO	40	E17	PGM0	PGM0
41	K18	Column I/O	Column I/O	42	F18	PGM2	PGM2
43	G19	nCSO	nCSO	44	F19	PGM1	PGM1
45	K19	Column I/O	Column I/O	46	K20	Column I/O	Column I/O
47	G20	CRC_ERROR	CRC_ERROR	48	F20	DATA1	DATA1
49	D21	DQ12T	DQ12T	50	C21	DQ11T	DQ11T
51	K21	Column I/O	Column I/O	52	J21	Column I/O	Column I/O
53	F22	DQ12T	DQ12T	54	E22	DQSn12T	DQSn12T
55	K22	Column I/O	Column I/O	56	J22	Column I/O	Column I/O
57	G23	DATA2	DATA2	58	F23	DQ12T	DQ12T
59	E24	DQ15T	DQ15T	60	C24	DQ13T	DQ13T
61	H24	RDYnBSY	RDYnBSY	62	E25	DQSn15T	DQSn15T
63	D26	DQ14T	DQ14T	64	C26	DQ14T	DQ14T
65	D27	DQ16T	DQ16T	66	C27	DQ16T	DQ16T
67	E28	DQ17T	DQ17T	68	C29	DQSn17T	DQSn17T
69	GND	GND	GND	70	GND	GND	GND

J6 Bank3 and Bank4							
PIN	PinOut	StratixII 180	StratixII 60	PIN	PinOut	StratixII 180	StratixII 60
1	GND	GND	GND	2	GND	GND	GND
3	C4	DQS0T	DQS0T	4	C5	DQSn0T	DQSn0T
5	D6	DQ1T	DQ1T	6	C6	DQ1T	DQ1T
7	D7	DQS2T	DQS2T	8	C7	DQSn2T	DQSn2T
9	F8	DQ4T	DQ4T	10	E8	DQ4T	DQ4T
11	F9	DQS4T/DQ0T	DQS4T/DQ0T	12	E9	DQSn4T	DQSn4T
13	G10	DQ6T	DQ6T	14	F10	DQ4T	DQ4T
15	D11	DQ5T	DQ5T	16	C11	DQSn5T	DQSn5T
17	H11	Column I/O	Column I/O	18	G11	DQ6T	DQ6T
19	G12	DQ6T	DQ6T	20	F12	DQSn6T	DQSn6T
21	E13	DQ8T	DQ8T	22	D13	DQ9T	DQ9T
23	J13	Column I/O	Column I/O	24	H13	Column I/O	Column I/O
25	H14	Column I/O	Column I/O	26	F14	DQS8T/DQ1T	DQS8T/DQ1T
27	E15	PLL5_FBn/OUT2n	PLL5_FBn/OUT2n	28	D15	PLL5_FBp/OUT2p	PLL5_FBp/OUT2p
29	L15	Column I/O	Column I/O	30	K15	Column I/O	Column I/O
31	L16	Column I/O	Column I/O	32	K16	Column I/O	Column I/O
33	VCC33	DC/DC POWER	DC/DC POWER	34	VCC33	DC/DC POWER	DC/DC POWER
35	GND	GND	GND	36	GND	GND	GND
37	VCCB34	VCCIO	VCCIO	38	VCCB34	VCCIO	VCCIO
39	E18	PLL11_OUT1n	PLL11_OUT1n	40	D18	PLL11_OUT1p	PLL11_OUT1p
41	E19	DQ10T	DQ10T	42	D19	DQS10T	DQS10T
43	J19	Column I/O	Column I/O	44	H19	DATA0	DATA0
45	E20	DQ10T	DQ10T	46	D20	DQSn10T	DQSn10T
47	J20	Column I/O	Column I/O	48	H20	Column I/O	Column I/O
49	H21	Column I/O	Column I/O	50	G21	Column I/O	Column I/O
51	D22	DQS12T/DQ2T	DQS12T/DQ2T	52	C22	DQ11T	DQ11T
53	H22	Column I/O	Column I/O	54	G22	Column I/O	Column I/O
55	D23	DQ12T	DQ12T	56	C23	DQ13T	DQ13T
57	J23	DATA4	DATA4	58	H23	DATA3	DATA3
59	G24	DATA7	DATA7	60	F24	DATA6	DATA6
61	D25	DQS15T/DQ7T	DQS15T/DQ7T	62	C25	DQ15T	DQ15T
63	E26	DQ15T	DQ15T	64	E27	DQ15T	DQ15T
65	D28	DQ17T	DQ17T	66	C28	DQS17T/DQ8T	DQS17T/DQ8T
67	C30	nCE	nCE	68	B31	DCLK	DCLK
69	GND	GND	GND	70	GND	GND	GND

J7 Bank5 and Bank6							
PIN	PinOut	StratixII 180	StratixII 60	PIN	PinOut	StratixII 180	StratixII 60
1	GND	GND	GND	2	GND	GND	GND
3	D3	FPLL10CLKp, Input	FPLL10CLKp, Input	4	D4	FPLL10CLKn, Input	FPLL10CLKn, Input
5	GND	GND	GND	6	VREF	VREF	VREF
7	D1	DIFFIO_RX111p	DIFFIO_RX43p	8	D2	DIFFIO_RX111n	DIFFIO_RX43n
9	E1	DIFFIO_RX113p	DIFFIO_RX45p	10	E2	DIFFIO_RX113n	DIFFIO_RX45n
11	F1	DIFFIO_RX115p	DIFFIO_RX47p	12	F2	DIFFIO_RX115n	DIFFIO_RX47n
13	G1	DIFFIO_RX117p	DIFFIO_RX49p	14	G2	DIFFIO_RX117n	DIFFIO_RX49n
15	H1	DIFFIO_RX119p	DIFFIO_RX51p	16	H2	DIFFIO_RX119n	DIFFIO_RX51n
17	J1	DIFFIO_RX120p	DIFFIO_RX52p	18	J2	DIFFIO_RX120n	DIFFIO_RX52n
19	K1	DIFFIO_RX122p	DIFFIO_RX54p	20	K2	DIFFIO_RX122n	DIFFIO_RX54n
21	L1	DIFFIO_RX126p	DIFFIO_RX58p	22	L2	DIFFIO_RX126n	DIFFIO_RX58n
23	M1	DIFFIO_RX128p	DIFFIO_RX60p	24	M2	DIFFIO_RX128n	DIFFIO_RX60n
25	P1	DIFFIO_RX130p	DIFFIO_RX62p	26	P2	DIFFIO_RX130n	DIFFIO_RX62n
27	R2	DIFFIO_RX129p	DIFFIO_RX61p	28	R3	DIFFIO_RX129n	DIFFIO_RX61n
29	T3	CLK11p, Input	CLK11p, Input	30	T4	CLK11n, Input	CLK11n, Input
31	T1	CLK10p/	CLK10p/	32	T2	CLK10n/	CLK10n/
33	VCC33	DC/DC POWER	DC/DC POWER	34	VCC33	DC/DC POWER	DC/DC POWER
35	GND	GND	GND	36	GND	GND	GND
37	VCCB56	VCCIO	VCCIO	38	VCCB56	VCCIO	VCCIO
39	U1	CLK8p/	CLK8p/	40	U2	CLK8n/	CLK8n/
41	U3	CLK9p, Input	CLK9p, Input	42	U4	CLK9n, Input	CLK9n, Input
43	V2	DIFFIO_RX131p	DIFFIO_RX63p	44	V3	DIFFIO_RX131n	DIFFIO_RX63n
45	W1	DIFFIO_RX132p	DIFFIO_RX64p	46	W2	DIFFIO_RX132n	DIFFIO_RX64n
47	AA1	DIFFIO_RX134p	DIFFIO_RX66p	48	AA2	DIFFIO_RX134n	DIFFIO_RX66n
49	AB1	DIFFIO_RX137p	DIFFIO_RX69p	50	AB2	DIFFIO_RX137n	DIFFIO_RX69n
51	AC1	DIFFIO_RX139p	DIFFIO_RX71p	52	AC2	DIFFIO_RX139n	DIFFIO_RX71n
53	AD1	DIFFIO_RX141p	DIFFIO_RX73p	54	AD2	DIFFIO_RX141n	DIFFIO_RX73n
55	AE1	DIFFIO_RX142p	DIFFIO_RX74p	56	AE2	DIFFIO_RX142n	DIFFIO_RX74n
57	AF1	DIFFIO_RX144p	DIFFIO_RX76p	58	AF2	DIFFIO_RX144n	DIFFIO_RX76n
59	AG1	DIFFIO_RX146p	DIFFIO_RX78p	60	AG2	DIFFIO_RX146n	DIFFIO_RX78n
61	AH1	DIFFIO_RX148p	DIFFIO_RX80p	62	AH2	DIFFIO_RX148n	DIFFIO_RX80n
63	AJ1	DIFFIO_RX150p	DIFFIO_RX82p	64	AJ2	DIFFIO_RX150n	DIFFIO_RX82n
65	GND	GND	GND	66	VREF	VREF	VREF
67	AJ3	FPLL9CLKp, Input	FPLL9CLKp, Input	68	AJ4	FPLL9CLKn, Input	FPLL9CLKn, Input
69	GND	GND	GND	70	GND	GND	GND

J8 Bank5 and Bank6							
PIN	PinOut	StratixII 180	StratixII 60	PIN	PinOut	StratixII 180	StratixII 60
1	GND	GND	GND	2	GND	GND	GND
3	E3	DIFFIO_RX112p	DIFFIO_RX44p	4	E4	DIFFIO_RX112n	DIFFIO_RX44n
5	G3	DIFFIO_RX116p	DIFFIO_RX48p	6	G4	DIFFIO_RX116n	DIFFIO_RX48n
7	H3	DIFFIO_RX110p	N.C.	8	H4	DIFFIO_RX110n	N.C.
9	J6	DIFFIO_TX109p	DIFFIO_TX42p	10	J7	DIFFIO_TX109n	DIFFIO_TX42n
11	K3	DIFFIO_RX121p	DIFFIO_RX53p	12	K4	DIFFIO_RX121n	DIFFIO_RX53n
13	K8	DIFFIO_TX112p	DIFFIO_TX44p	14	K9	DIFFIO_TX112n	DIFFIO_TX44n
15	L5	DIFFIO_TX116p	DIFFIO_TX48p	16	L6	DIFFIO_TX116n	DIFFIO_TX48n
17	L9	DIFFIO_TX114p	DIFFIO_TX45p	18	L10	DIFFIO_TX114n	DIFFIO_TX45n
19	M6	DIFFIO_TX119p	DIFFIO_TX51p	20	M7	DIFFIO_TX119n	DIFFIO_TX51n
21	N2	DIFFIO_RX127p	DIFFIO_RX59p	22	N3	DIFFIO_RX127n	DIFFIO_RX59n
23	N6	DIFFIO_TX120p	DIFFIO_TX52p	24	N7	DIFFIO_TX120n	DIFFIO_TX52n
25	P4	DIFFIO_TX124p	DIFFIO_TX56p	26	P5	DIFFIO_TX124n	DIFFIO_TX56n
27	P8	DIFFIO_TX122p	DIFFIO_TX54p	28	P9	DIFFIO_TX122n	DIFFIO_TX54n
29	R6	DIFFIO_TX126p	DIFFIO_TX58p	30	R7	DIFFIO_TX126n	DIFFIO_TX58n
31	T5	DIFFIO_TX129p	DIFFIO_TX61p	32	T6	DIFFIO_TX129n	DIFFIO_TX61n
33	VCC33	DC/DC POWER	DC/DC POWER	34	VCC33	DC/DC POWER	DC/DC POWER
35	GND	GND	GND	36	GND	GND	GND
37	VCCB56	VCCIO	VCCIO	38	VCCB56	VCCIO	VCCIO
39	U5	DIFFIO_TX131p	DIFFIO_TX63p	40	U6	DIFFIO_TX131n	DIFFIO_TX63n
41	V4	DIFFIO_TX135p	DIFFIO_TX67p	42	V5	DIFFIO_TX135n	DIFFIO_TX67n
43	V9	DIFFIO_TX133p	DIFFIO_TX65p	44	V10	DIFFIO_TX133n	DIFFIO_TX65n
45	W6	DIFFIO_TX137p	DIFFIO_TX69p	46	W7	DIFFIO_TX137n	DIFFIO_TX69n
47	Y2	DIFFIO_RX133p	DIFFIO_RX65p	48	Y3	DIFFIO_RX133n	DIFFIO_RX65n
49	Y6	DIFFIO_TX139p	DIFFIO_TX71p	50	Y7	DIFFIO_TX139n	DIFFIO_TX71n
51	AA3	DIFFIO_RX135p	DIFFIO_RX67p	52	AA4	DIFFIO_RX135n	DIFFIO_RX67n
53	AA8	DIFFIO_TX145p	DIFFIO_TX78p	54	AA9	DIFFIO_TX145n	DIFFIO_TX78n
55	AB5	DIFFIO_TX146p	DIFFIO_TX74p	56	AB6	DIFFIO_TX146n	DIFFIO_TX74n
57	AB9	DIFFIO_TX147p	DIFFIO_TX81p	58	AB10	DIFFIO_TX147n	DIFFIO_TX81n
59	AC6	DIFFIO_TX150p	DIFFIO_TX79p	60	AC7	DIFFIO_TX150n	DIFFIO_TX79n
61	AD3	DIFFIO_RX145p	N.C.	62	AD4	DIFFIO_RX145n	N.C.
63	AD8	DIFFIO_TX151p	DIFFIO_TX83p	64	AD9	DIFFIO_TX151n	DIFFIO_TX83n
65	AE5	DIFFIO_RX149p	N.C.	66	AE6	DIFFIO_RX149n	N.C.
67	AG3	DIFFIO_RX151p	DIFFIO_RX79p	68	AG4	DIFFIO_RX151n	DIFFIO_RX79n
69	GND	GND	GND	70	GND	GND	GND

J9 Bank5 and Bank6							
PIN	PinOut	StratixII 180	StratixII 60	PIN	PinOut	StratixII 180	StratixII 60
1	GND	GND	GND	2	GND	GND	GND
3	F3	DIFFIO_RX114p	DIFFIO_RX46p	4	F4	DIFFIO_RX114n	DIFFIO_RX46n
5	G5	DIFFIO_RX109p	N.C.	6	G6	DIFFIO_RX109n	N.C.
7	J3	DIFFIO_RX118p	DIFFIO_RX50p	8	J4	DIFFIO_RX118n	DIFFIO_RX50n
9	J8	DIFFIO_TX110p	DIFFIO_TX43p	10	J9	DIFFIO_TX110n	DIFFIO_TX43n
11	K6	DIFFIO_TX111p	DIFFIO_TX47p	12	K7	DIFFIO_TX111n	DIFFIO_TX47n
13	L3	DIFFIO_RX123p	DIFFIO_RX55p	14	L4	DIFFIO_RX123n	DIFFIO_RX55n
15	L7	DIFFIO_TX113p	DIFFIO_TX46p	16	L8	DIFFIO_TX113n	DIFFIO_TX46n
17	M3	DIFFIO_RX125p	DIFFIO_RX57p	18	M4	DIFFIO_RX125n	DIFFIO_RX57n
19	M8	DIFFIO_TX115p	DIFFIO_TX50p	20	M9	DIFFIO_TX115n	DIFFIO_TX50n
21	N4	DIFFIO_RX124p	DIFFIO_RX56p	22	N5	DIFFIO_RX124n	DIFFIO_RX56n
23	N8	DIFFIO_TX121p	DIFFIO_TX53p	24	N9	DIFFIO_TX121n	DIFFIO_TX53n
25	P6	DIFFIO_TX123p	DIFFIO_TX55p	26	P7	DIFFIO_TX123n	DIFFIO_TX55n
27	R4	DIFFIO_TX127p	DIFFIO_TX59p	28	R5	DIFFIO_TX127n	DIFFIO_TX59n
29	R10	DIFFIO_TX128p	DIFFIO_TX60p	30	R11	DIFFIO_TX128n	DIFFIO_TX60n
31	T10	DIFFIO_TX130p	DIFFIO_TX62p	32	T11	DIFFIO_TX130n	DIFFIO_TX62n
33	VCC33	DC/DC POWER	DC/DC POWER	34	VCC33	DC/DC POWER	DC/DC POWER
35	GND	GND	GND	36	GND	GND	GND
37	VCCB56	VCCIO	VCCIO	38	VCCB56	VCCIO	VCCIO
39	U10	DIFFIO_TX132p	DIFFIO_TX64p	40	U11	DIFFIO_TX132n	DIFFIO_TX64n
41	V6	DIFFIO_TX134p	DIFFIO_TX66p	42	V7	DIFFIO_TX134n	DIFFIO_TX66n
43	W4	DIFFIO_TX138p	DIFFIO_TX70p	44	W5	DIFFIO_TX138n	DIFFIO_TX70n
45	W8	DIFFIO_TX136p	DIFFIO_TX68p	46	W9	DIFFIO_TX136n	DIFFIO_TX68n
47	Y4	DIFFIO_RX136p	DIFFIO_RX68p	48	Y5	DIFFIO_RX136n	DIFFIO_RX68n
49	Y8	DIFFIO_TX140p	DIFFIO_TX72p	50	Y9	DIFFIO_TX140n	DIFFIO_TX72n
51	AA6	DIFFIO_TX142p	DIFFIO_TX76p	52	AA7	DIFFIO_TX142n	DIFFIO_TX76n
53	AB3	DIFFIO_RX138p	DIFFIO_RX70p	54	AB4	DIFFIO_RX138n	DIFFIO_RX70n
55	AB7	DIFFIO_TX148p	DIFFIO_TX80p	56	AB8	DIFFIO_TX148n	DIFFIO_TX80n
57	AC3	DIFFIO_RX140p	DIFFIO_RX72p	58	AC4	DIFFIO_RX140n	DIFFIO_RX72n
59	AC8	DIFFIO_TX149p	DIFFIO_TX82p	60	AC9	DIFFIO_TX149n	DIFFIO_TX82n
61	AD6	DIFFIO_TX152p	DIFFIO_TX77p	62	AD7	DIFFIO_TX152n	DIFFIO_TX77n
63	AE3	DIFFIO_RX143p	DIFFIO_RX75p	64	AE4	DIFFIO_RX143n	DIFFIO_RX75n
65	AF3	DIFFIO_RX147p	DIFFIO_RX77p	66	AF4	DIFFIO_RX147n	DIFFIO_RX77n
67	AH3	DIFFIO_RX152p	DIFFIO_RX81p	68	AH4	DIFFIO_RX152n	DIFFIO_RX81n
69	GND	GND	GND	70	GND	GND	GND

J10 Bank7 and Bank8							
PIN	PinOut	StratixII 180	StratixII 60	PIN	PinOut	StratixII 180	StratixII 60
1	GND	GND	GND	2	GND	GND	GND
3	AM4	DQ0B	DQ0B	4	AL4	DQ0B	DQ0B
5	GND	GND	GND	6	VREF	VREF	VREF
7	AM5	DQ2B	DQ2B	8	AL5	DQS2B	DQS2B
9	AM6	DQ2B	DQ2B	10	AL6	DQSn2B	DQSn2B
11	AM7	DQ3B	DQ3B	12	AL7	DQS3B/DQ1B	DQS3B/DQ1B
13	AM8	DQ3B	DQ3B	14	AL8	DQSn3B	DQSn3B
15	AM9	DQ4B	DQ4B	16	AL9	DQSn4B	DQSn4B
17	AM10	DQ6B	DQ6B	18	AL10	DQ6B	DQ6B
19	AM11	DQ7B	DQ7B	20	AL11	DQS7B/DQ3B	DQS7B/DQ3B
21	AM12	DQ7B	DQ7B	22	AL12	DQSn7B	DQSn7B
23	AL13	DQSn9B	DQSn9B	24	AK13	DQS9B/DQ4B	DQS9B/DQ4B
25	AM14	DQ9B	DQ9B	26	AL14	DQ9B	DQ9B
27	AL15	PLL6_FBp/OUT2p	PLL6_FBp/OUT2p	28	AK15	PLL6_FBn/OUT2n	PLL6_FBn/OUT2n
29	AH16	CLK7p	CLK7p	30	AG16	CLK7n	CLK7n
31	AM16	CLK6p	CLK6p	32	AL16	CLK6n	CLK6n
33	VCC33	DC/DC POWER	DC/DC POWER	34	VCC33	DC/DC POWER	DC/DC POWER
35	GND	GND	GND	36	GND	GND	GND
37	VCCB78	VCCIO	VCCIO	38	VCCB78	VCCIO	VCCIO
39	AM17	CLK4p	CLK4p	40	AL17	CLK4n	CLK4n
41	AK17	CLK5p	CLK5p	42	AJ17	CLK5n	CLK5n
43	AL18	PLL12_OUT0p	PLL12_OUT0p	44	AK18	PLL12_OUT0n	PLL12_OUT0n
45	AM19	PLL12_FBp/OUT2p	PLL12_FBp/OUT2p	46	AL19	PLL12_FBn/OUT2n	PLL12_FBn/OUT2n
47	AL20	DQ10B	DQ10B	48	AK20	DQS10B	DQS10B
49	AM21	DQ11B	DQ11B	50	AL21	DQS11B/DQ5B	DQS11B/DQ5B
51	AM22	DQ11B	DQ11B	52	AL22	DQSn11B	DQSn11B
53	AM23	DQ13B	DQ13B	54	AL23	DQS13B/DQ6B	DQS13B/DQ6B
55	AM24	DQ13B	DQ13B	56	AL24	DQSn13B	DQSn13B
57	AM25	DQ15B	DQ15B	58	AL25	DQS15B/DQ7B	DQS15B/DQ7B
59	AM26	DQ15B	DQ15B	60	AL26	DQSn15B	DQSn15B
61	AM27	DQ16B	DQ16B	62	AL27	DQS16B/DQ3B	DQS16B/DQ3B
63	AM28	DQ16B	DQ16B	64	AL28	DQSn16B	DQSn16B
65	GND	GND	GND	66	VREF	VREF	VREF
67	AM29	DQ17B	DQ17B	68	AL29	DQ17B	DQ17B
69	GND	GND	GND	70	GND	GND	GND

J11 Bank7 and Bank8							
PIN	PinOut	StratixII 180	StratixII 60	PIN	PinOut	StratixII 180	StratixII 60
1	GND	GND	GND	2	GND	GND	GND
3	AK3	nIO_PULLUP	nIO_PULLUP	4	AK4	DQS0B	DQS0B
5	AH6	DQ1B	DQ1B	6	AH5	DQ0B	DQ0B
7	AK7	DQ3B	DQ3B	8	AJ7	DQ3B	DQ3B
9	AJ8	DQ4B	DQ4B	10	AH8	DQSn1B	DQSn1B
11	AK9	DQS4B/DQ0B	DQS4B/DQ0B	12	AH9	DQ1B	DQ1B
13	AG10	DQ5B	DQ5B	14	AF10	DQ5B	DQ5B
15	AD11	Column I/O	Column I/O	16	AC11	Column I/O	Column I/O
17	AH11	DQ6B	DQ6B	18	AG11	DQSn5B	DQSn5B
19	AE12	Column I/O	Column I/O	20	AD12	Column I/O	Column I/O
21	AK12	DQ7B	DQ7B	22	AJ12	DQ7B	DQ7B
23	AG13	DQ8B	DQ8B	24	AF13	DQ8B	DQ8B
25	AD14	Column I/O	Column I/O	26	AC14	Column I/O	Column I/O
27	AJ14	DQ9B	DQ9B	28	AH14	DQSn8B	DQSn8B
29	AJ15	PLL6_OUT1p	PLL6_OUT1p	30	AH15	PLL6_OUT1n	PLL6_OUT1n
31	AK16	PLL6_OUT0p	PLL6_OUT0p	32	AJ16	PLL6_OUT0n	PLL6_OUT0n
33	VCC33	DC/DC POWER	DC/DC POWER	34	VCC33	DC/DC POWER	DC/DC POWER
35	GND	GND	GND	36	GND	GND	GND
37	VCCB78	VCCIO	VCCIO	38	VCCB78	VCCIO	VCCIO
39	AC17	Column I/O	Column I/O	40	AB17	Column I/O	Column I/O
41	AD18	Column I/O	Column I/O	42	AC18	Column I/O	Column I/O
43	AD19	Column I/O	Column I/O	44	AC19	Column I/O	Column I/O
45	AG19	DEV_CLRn	DEV_CLRn	46	AE19	Column I/O	Column I/O
47	AD20	Column I/O	Column I/O	48	AC20	Column I/O	Column I/O
49	AH20	DQ10B	DQ10B	50	AG20	Column I/O	Column I/O
51	AE21	Column I/O	Column I/O	52	AD21	Column I/O	Column I/O
53	AE22	Column I/O	Column I/O	54	AD22	Column I/O	Column I/O
55	AJ22	DQS12B/DQ2B	DQS12B/DQ2B	56	AH22	DQSn12B	DQSn12B
57	AE23	nWS	nWS	58	AD23	CLKUSR	CLKUSR
59	AK24	DQ13B	DQ13B	60	AJ23	DQ12B	DQ12B
61	AH24	DQ14B	DQ14B	62	AG24	DQ14B	DQ14B
63	AJ25	DQS14B	DQS14B	64	AH25	DQSn14B	DQSn14B
65	AK27	DQ16B	DQ16B	66	AJ27	DQ16B	DQ16B
67	AK29	DQSn17B	DQSn17B	68	AK28	DQS17B/DQ8B	DQS17B/DQ8B
69	GND	GND	GND	70	GND	GND	GND

J12 Bank7 and Bank8							
PIN	PinOut	StratixII 180	StratixII 60	PIN	PinOut	StratixII 180	StratixII 60
1	GND	GND	GND	2	GND	GND	GND
3	AL2	PORSEL	PORSEL	4	AL3	nCEO	nCEO
5	AK5	DQSn0B	DQSn0B	6	AJ5	DQ0B	DQ0B
7	AK6	DQ2B	DQ2B	8	AJ6	DQ2B	DQ2B
9	AK8	DQ4B	DQ4B	10	AH7	DQ1B	DQ1B
11	AG9	DQ1B	DQ1B	12	AG8	DQS1B/DQ0B	DQS1B/DQ0B
13	AE10	Column I/O	Column I/O	14	AD10	RUP7	RUP7
15	AK10	DQS6B	DQS6B	16	AJ10	DQ4B	DQ4B
17	AF11	DQS5B/DQ2B	DQS5B/DQ2B	18	AE11	Column I/O	Column I/O
19	AK11	DQSn6B	DQSn6B	20	AJ11	DQ6B	DQ6B
21	AG12	DQ5B	DQ5B	22	AF12	DQ5B	DQ5B
23	AE13	Column I/O	Column I/O	24	AD13	Column I/O	Column I/O
25	AJ13	DQ9B	DQ9B	26	AH13	DQ8B	DQ8B
27	AG14	DQS8B/DQ1B	DQS8B/DQ1B	28	AE14	Column I/O	Column I/O
29	AG15	DQ8B	DQ8B	30	AC15	Column I/O	Column I/O
31	AC16	Column I/O	Column I/O	32	AB16	Column I/O	Column I/O
33	VCC33	DC/DC POWER	DC/DC POWER	34	VCC33	DC/DC POWER	DC/DC POWER
35	GND	GND	GND	36	GND	GND	GND
37	VCCB78	VCCIO	VCCIO	38	VCCB78	VCCIO	VCCIO
39	AH17	DEV_OE	DEV_OE	40	AG17	RUnLU	RUnLU
41	AJ18	PLL12_OUT1p	PLL12_OUT1p	42	AH18	PLL12_OUT1n	PLL12_OUT1n
43	AF19	Column I/O	Column I/O	44	AG18	nCS	nCS
45	AJ19	DQ10B	DQ10B	46	AH19	DQ10B	DQ10B
47	AF20	Column I/O	Column I/O	48	AE20	Column I/O	Column I/O
49	AK21	DQ11B	DQ11B	50	AJ20	DQSn10B	DQSn10B
51	AJ21	DQ11B	DQ11B	52	AF21	Column I/O	Column I/O
53	AG22	DQ12B	DQ12B	54	AF22	Column I/O	Column I/O
55	AK23	DQ13B	DQ13B	56	AK22	DQ12B	DQ12B
57	AG23	DQ12B	DQ12B	58	AF23	nRS	nRS
59	AF24	TCK	TCK	60	AE24	TMS	TMS
61	AK26	DQ15B	DQ15B	62	AK25	DQ14B	DQ14B
63	AJ26	DQ15B	DQ15B	64	AH26	DQ14B	DQ14B
65	AJ28	DQ17B	DQ17B	66	AH28	DQ17B	DQ17B
67	AL31	TDI	TDI	68	AK30	TRST	TRST
69	GND	GND	GND	70	GND	GND	GND

Chapter 3

Electrical and Mechanical Specifications

This chapter describes the important Electrical and Mechanical specifications of TREX-S2, including how to plug or unplug the TREX-S2 from its associated main boards.

Operation and Environment Condition

This section describes the electrical specifications of TREX-S2

- ✓ Input Voltage: *3.3V ±10%*
- ✓ Input Current: *FPGA 3.3V I/O current + 1.8V I/O current * 0.6 + 1.2V core current * 0.4.*
- ✓ Power Consumption: *(FPGA 3.3V I/O current + 1.8V I/O current * 0.6 + 1.2V core current * 0.4) * 3.3V*. (Please use the heatsink attached to ensure a stable working temperature.
- ✓ **Configuration default setup**:
  - ■ **nIO_PULLUP** is low (via a 4.7K pull-down resistor)
  - ■ **PORSEL** is low (via a 4.7K pull-down resistor)
  - ■ **MSEL0 – MSEL3** is floating (users' main board must connect these pins to **HIGH** or **LOW** according to the preferred configuration method selected)
- ✓ Power Supplier Mechanism
  - ■ VCCINT: Generated power supply at 1.2V @ 6A~18A (6A for EP2S60, 12A for EP2S180 and 18A is reserved)

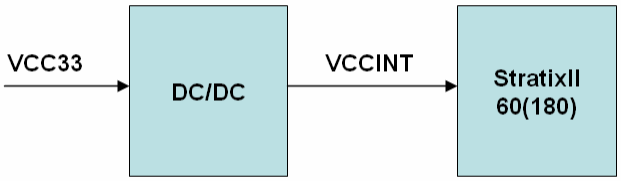

Figure 3.1: The Generation of VCCINT on TREX-S2

TREX-S2 Mechanical Description

The following diagram shows the mechanical diagram of the TREX-S2 module. The complete diagram is also included in the CD-ROM included.

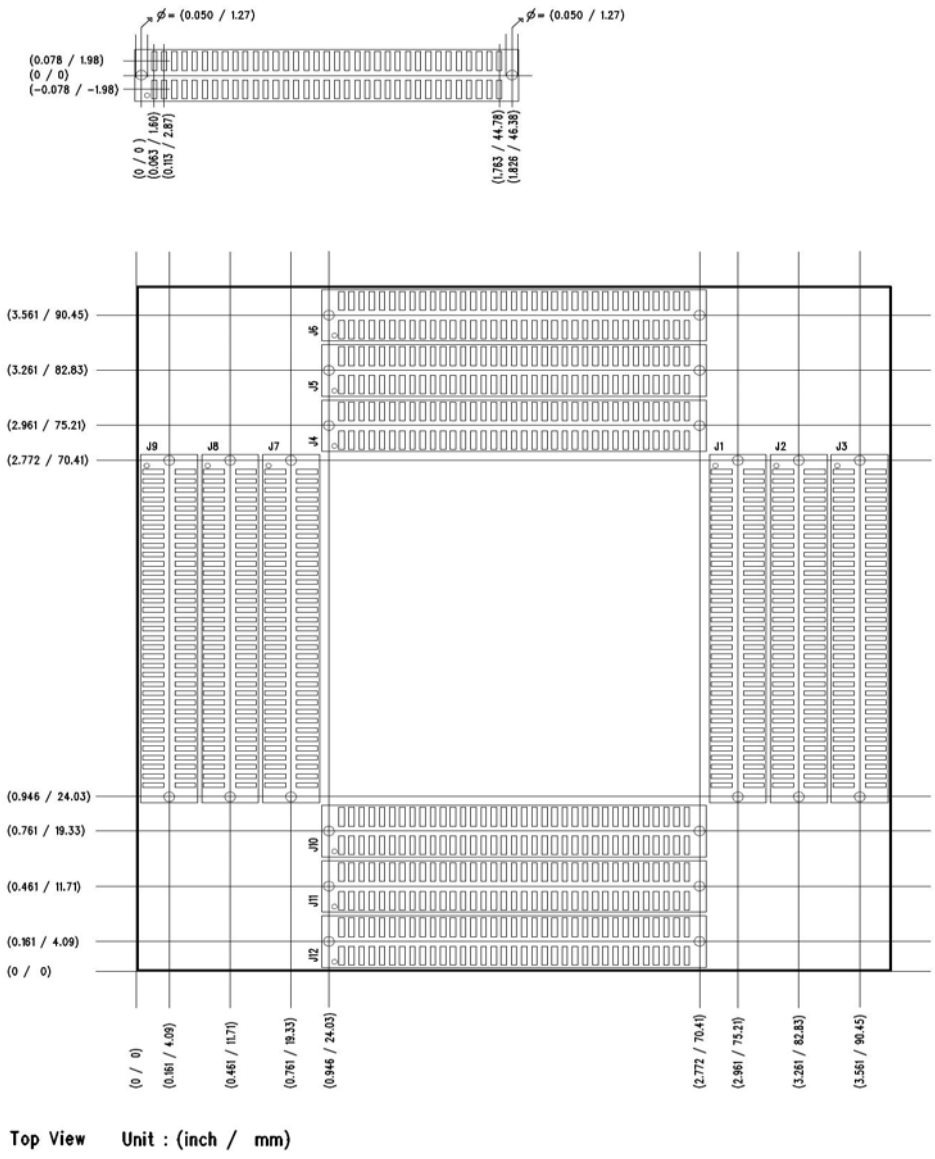

Figure 3.2 The TREX-S2 mechanical diagram

Motherboard Design Guide for Easy Installation

TREX-S2 has 12 connectors for connecting itself to a motherboard. It is very difficult to unplug the module once it is installed on a motherboard. Therefore, we designed a tool to allow users to easily unplug the module from the motherboard. Please refer to Figure 3.3 for the Terasic FPGA Module Opener.

- ✓ Note that when you design your own motherboards, you need to reserve enough empty space around the connectors for the opener's stand. Please refer to **TREX-S2-TMA** spec, where we provide schematic and gerber files free to our customers to shorten their design cycle.
- ✓ **Please refer to the TS2withMotherboard.pdf to get more detailed steps about how to connect and detach the TREX-S2 FPGA module with TREX-S2-TMA/TMB motherboard.**

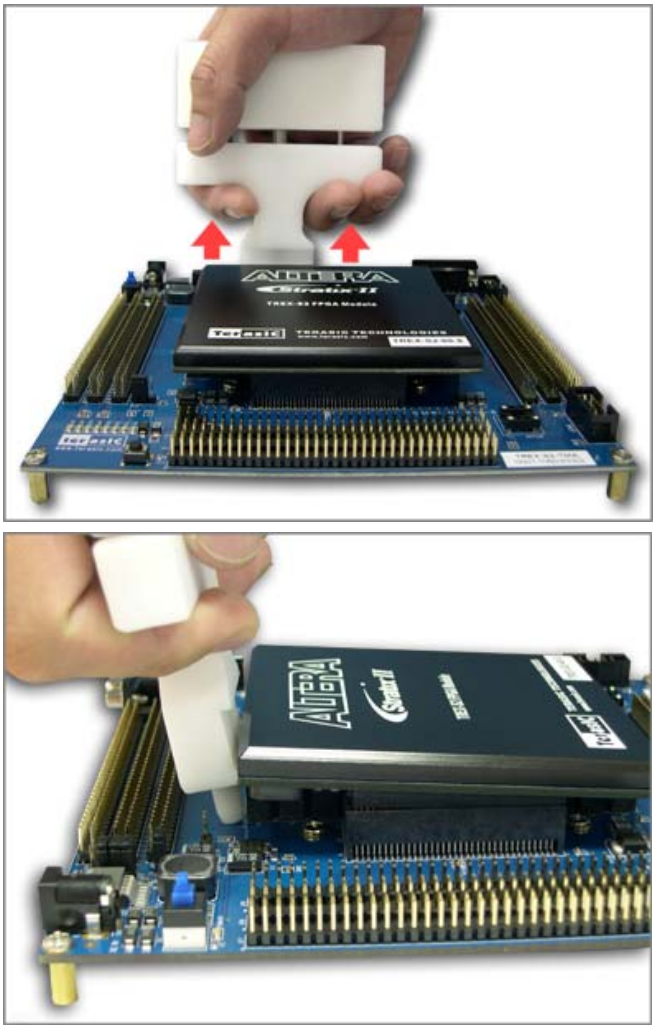

Figure 3.3 Use the Terasic FPGA Module Opener to unplug the TREX-S2 board

Chapter 4

Appendix

Revision History

Date	Change Log
Mar 23, 2006 (SP)	Initial Version
Aug 15, 2006 (JC)	Update for v1.2 PCB

Part Number of Component on Board

For EP2S60 (v1.1 PCB)

Component Type	Manufacturer	Vender Part Number	Reference
IC	ALTERA	EPCS16SI16N	U4
IC	PERICOM	PI3VT3245LE	U5
Connector	SAMTEC	SFC-135-T2-L-D-A	J1~J12

For EP2S60 and EP2S180 (v1.2 PCB)

Component Type	Manufacturer	Vender Part Number	Reference
IC	ALTERA	EPCS16SI16N	U2 (For EP2S60)
IC	ALTERA	EPCS64SI16N	U2 (For EP2S180)
IC	PERICOM	PI3VT3245LE	U3
Connector	SAMTEC	SFC-135-T2-L-D-A	J1~J12

Always Visit TREX-S2 Webpage for New Main board

We will be continuing creating various main board and labs on our DE2 webpage. Please visit **TREXS2.terasic.com** for more information.